TNG New Generation CCD Controller

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Abstract: The CCD manufacturers have improved the scientific CCDs in terms of number of pixels, readout speed and noise. 4K×4K 2 output CCDs are currently available and show a readout noise less than 5 electrons r.m.s. at a readout speed of 1 Mpixel/s. To take full advantage of the CCD technology improvements an "up-to-date" CCD controller will be needed. For this reason, at the TNG, we have decided to design a new CCD controller able to drive quickly large area CCDs as well as mosaics without degrading the readout noise allowed by these new CCDs. In this paper we describe briefly the design and present the expected performances.

1. INTRODUCTION

At the Telescopio Nazionale Galileo (TNG), the Italian national facility located at Roque de los Muchachos in La Palma (Canary Islands, Spain), three scientific instruments, having CCDs as detectors, will carry out photometric and spectrographic observations. One of those, that currently is working, is the optical imager (OIG) that has a mosaic of two 2K×4K EEV 42-80 CCDs. The other two that will be in operation in mid-2000 are the low resolution spectrograph (LRS) equipped with a 2K×2K LORAL CCD and the high resolution spectrograph (SARG) equipped with a mosaic of two 2K×4K EEV 4280 CCDs [3].

In order to read the two EEV chips of the OIG, our CCD controller, developed a long time ago [1], [2], allows the whole image to be read in about 250 seconds. This speed, of course, is not adequate for the current readout allowed by new CCDs.

To take full advantage of the improvements in CCD technology, a new CCD controller has been designed. This controller is able to quickly drive large-area CCDs as well as mosaics without degrading the readout noise. The compactness, weight, readout speed and the noise performance are the key points that have moulded the design. The idea is to provide all digital sequences for the CCDs, from an interface located on the host computer, and connect to this the CCD electronics through a high speed full duplex fibre link.

With a Correlated Double Sampler (CDS) of 2.5 μs at minimum, this new CCD controller will allow an acquisition rate of 400 kpixels/s per channel, and thanks to the high speed link, many channels will be read at a speed which is very useful for large mosaics.

2. THE CCD CONTROLLER

As stated above, the CCD controller design is driven by the idea to have, on board the host computer interface, all the electronics that generate the digital signals as well as the sequences generator that is a Digital Signal Processor (DSP). The signals will be replicated on the SEQUENCER board that also provides the clocks to the CCD(s). In fact, the board has digital-to-analog converters for the upper and lower level voltages of the clocks.

We adopted the PCI bus standard to interface the CCD controller to the host computer. The AMCC S5933 PCI matchmaker controller chip is used for this purpose.

To handle the incoming data we use a FIFO memory and the AMCC S5933 chip. The data rate on the bus is 33 Mwords/sec (32 bits wide words) and a Win 9X, Win NT driver has been developed to store the data pixel on the PC memory.

The CCD controller, aside from the power supply, is made up essentially of three electronic boards: two double Euro-card and one extended PCI board. Figure 1 shows a schematic diagram of all the architecture.

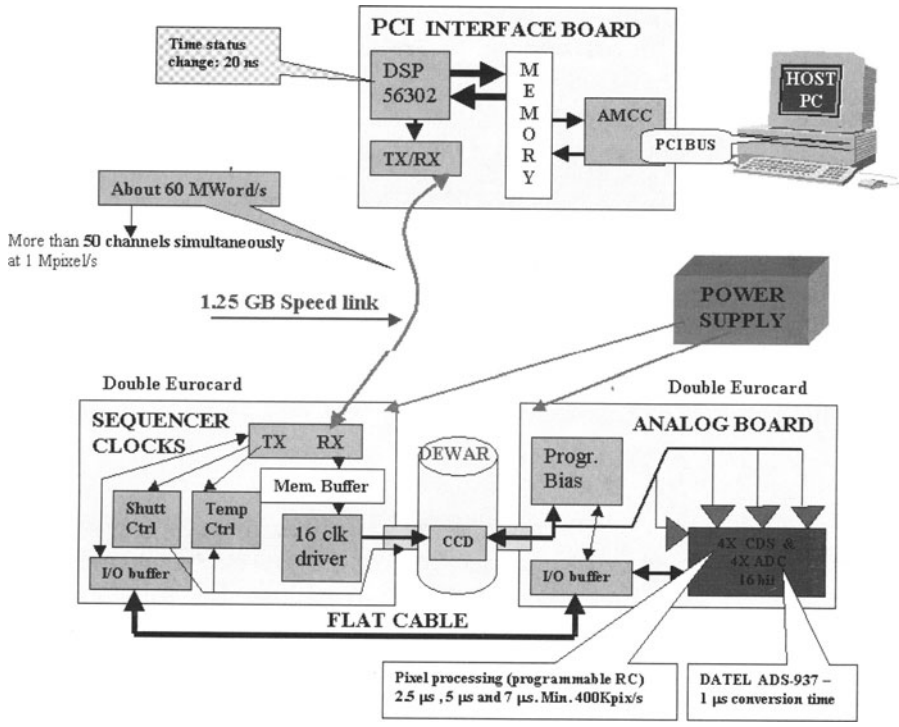

Figure 1. Block Diagram on the CCD Controller

The three boards are:

1. A PCI board based on the DSP Motorola 56302 that provides all digital sequences to drive CCDs. An AMCC S5933 PCI controller is used to interface the PCI bus. A transmitter/receiver chip set constituted by the HDMP 1022 (21 bits data parallel-to-serial) and the HDMP1024 (21 bits serial-to-parallel) manufactured by HP. A fibre optic provides a fast link with the two other boards.
2. A CCD Sequencer Board/Clock driver that receives all sequences from the PCI board and replicate the signals delivered by the DSP. This board also provides all the signals needed to generate 16 clocks.
3. An Analog Board that provides 8 programmable bias voltages and processing and acquisition of four different video channels. The Correlated Double Sampling (CDS) technique has been adopted, and three different integration times can be selected from 7 to 2.5 µs. Furthermore each analog board is able to host four 16 bits Datel ADS 937 ADCs (conversion time of 1 µs). A sequencer board and a PCI interface can

handle simultaneously up to 8 analog boards, and thus up to 32 analog channels can be treated simultaneously.

This architecture, by using just two thin boxes connected directly to the CCD dewar, is capable of driving a mosaic of four CCDs (one output) or a mosaic of two CCDs (two outputs). Only two fibres are required to link the CCD controller to the host computer, one to send digital sequences and commands, and the other to receive data. A flat cable is used to connect the analog box to the sequencer box; the processed and converted pixel signal will be sent to the host interface through the transmitter (HDMP 1022) on board the sequencer.

3. EXPECTED PERFORMANCES

From a mechanical point of view, the system will be very compact. As stated earlier, just two thin boxes will be connected directly to the dewar and no other cabling, except for a fibre and few wires for power supply, is required.

From an electronic point of view, the system becomes less noise-sensitive because all analog electronics are close to the CCD. And thanks to this unique architecture we are encouraged to use switching power supply instead of the linear ones. We are confident that this architecture will have a high noise rejection and will be able to maintain the noise performance of the currently available CCDs.

As said in the previous section, a PCI interface and a sequencer together can drive 8 analog boards simultaneously and thus, a maximum of 32 channels can be acquired at one time. This means that it is possible to drive a mosaic of 16 CCDs (two outputs). To acquire a further 32 channels, another sequencer and another PCI interface will be required. The high-speed link is capable to sustain 64 channels at a rate of 400 kpixels/s, and thus the configured system could handle all the channels without any degradation of acquisition time. Table 1 shows some possible configurations for 2K×4K CCDs. The achievable total read time (selecting an integration time of 2.5 μs) for the various composed mosaics is computed and reported in the fourth column. As can be seen, at a data rate of 400 kpixel/s, the total read time is not affected by the link.